

Amendment to the claims

Please amend claims 1-13 as shown in the following listing of claims.
This listing of claims will replace all prior versions, and listings, of claims in the
5 application.

- 1 1. (currently amended) A receiver (~~RECEP~~) for receiving an input signal
2 comprising a series of samples (~~IN_TIME, EARLY, LATE, VOID~~), said receiver
3 (~~RECEP~~) comprising one delay line (~~D_LINE~~), characterized in that the delay line
4 (~~D_LINE~~) is intended configured to delay said input signal by a series of delays
5 (τ) and is divided into a series of delay sub-lines (~~ZONE~~) each intended being
6 used to write one from the series of samples (~~IN_TIME, EARLY, LATE, VOID~~)
7 of said input signal (~~INPUT~~), each of the delay sub-lines including a memory area
8 to receive at least one sample from the series of samples, and in that the solution
9 further comprises control means (~~RD_ADD_GEN~~) intended configured to
10 generate read addresses of the samples in the delay sub-lines (~~ZONE~~) from the
11 series of samples (~~IN_TIME, EARLY, LATE, VOID~~) of the input signal
12 (~~INPUT~~), so that a read address is equal to a difference between a write address of
13 a sample in a delay sub-line (~~ZONE~~) of the input signal and a delay (τ) expressed
14 as a number of sampling periods from the series of delays (τ).
- 1 2. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that the delay line comprises a single series of delay sub-lines.
- 1 3. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that the delay line comprises various series (~~BANK~~) of delay sub-
3 lines.
- 1 4. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that a delay sub-line (~~ZONE~~) is accessible with a frequency twice
3 as fast as the samples of an input signal received by the receiver (~~RECEP~~).

1 5. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that one memory area is associated to one delay sub-line (~~ZONE~~).

1 6. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that the samples of a series of samples (~~IN_TIME, EARLY,~~
3 ~~LATE, VOID~~) are accessible in parallel in the write mode or read mode in the
4 delay sub-lines (~~ZONE~~).

1 7. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that the read addresses of the samples of a series of samples
3 (~~IN_TIME, EARLY, LATE, VOID~~) are situated at addresses immediately
4 adjacent or equal to one another.

1 8. (currently amended) A receiver (~~RECEP~~) as claimed in claim 3,
2 characterized in that two series of samples (~~C_CHIP, NEXT_CHIP~~) are read in
3 parallel.

1 9. (currently amended) A receiver (~~RECEP~~) as claimed in the preceding
2 claim 8, characterized in that the delay line (~~D_LINE~~) comprises selection means
3 (~~SELECT_BANK~~) of a series (~~BANK~~) of delay sub-lines to which belongs one of
4 the two series of samples read as a function of the delay (τ).

1 10. (currently amended) A receiver (~~RECEP~~) as claimed in claim 1,
2 characterized in that the delay line (~~D_LINE~~) comprises a position factor
3 (~~DOWN_POS~~) indicating the position of a reference sample (~~IN_TIME~~) from a
4 series of samples (~~IN_TIME, EARLY, LATE, VOID~~) of an input signal in the
5 series of delay sub-lines to which it belongs.

1 11. (currently amended) A receiver (~~RECEP~~) as claimed in the preceding
2 claim 8, characterized in that the memory areas (~~ZONE~~) are regrouped into a first
3 and a second group (~~GROUPEA, GROUPEB~~), the first group regrouping a
4 current series of current areas (~~C_BANK~~) and a next series of areas
5 (~~NEXT_BANK~~) which can each correspond to the first series (~~BANK0~~) of delay
6 sub-lines and the second group regrouping a current series of areas (~~C_BANK~~)
7 and a next series of areas (~~NEXT_BANK~~) which can each correspond to the
8 second series (~~BANK1~~) of the delay sub-lines, so that the memory areas for a
9 series of samples read are identical for each equal position factor value
10 (~~DOWN_POS~~).

1 12. (currently amended) A delay line (~~D_LINE~~) for delaying an input signal
2 (~~INPUT~~), said input signal comprising a series of samples, (~~IN_TIME, EARLY,~~
3 ~~LATE, VOID~~), characterized in that the delay line is ~~intended~~ configured to delay
4 said input signal by a series of delays (τ) and is divided into a series of delay sub-
5 lines (~~ZONE~~) each ~~intended~~ being used to write one from the series of samples
6 (~~IN_TIME, EARLY, LATE, VOID~~) of said input signal (~~INPUT~~), each of the
7 delay sub-lines including a memory area to receive at least one sample from the
8 series of samples, and in that the delay line comprises control means
9 (~~RD_ADD_GEN~~) ~~intended~~ configured to generate read addresses of the samples
10 in the delay sub-lines (~~ZONE~~) from the series of samples (~~IN_TIME, EARLY,~~
11 ~~LATE, VOID~~) of the input signal (~~INPUT~~), so that a read address is equal to a
12 difference between a write address of a sample in a delay sub-line (~~ZONE~~) of the
13 input signal and a delay (τ) expressed as a number of sampling periods of the
14 series of delays (τ).

1 13. (currently amended) A method of delaying an input signal ~~(INPUT)~~ by
2 means of a delay line ~~(D_LINE)~~, said input signal comprising a series of samples
3 ~~(IN_TIME, EARLY, LATE)~~, characterized in that it comprises the steps of:
4 dividing the delay line ~~(D_LINE)~~ into a series of delay sub-lines
5 ~~(ZONE)~~ each ~~intended~~ configured to receive a sample from the series of samples
6 ~~(IN_TIME, EARLY, LATE, VOID)~~ of the input signal ~~(INPUT)~~, each of the
7 delay sub-lines including a memory area to receive the sample, said delay line
8 being ~~intended~~ configured to delay said input signal by a series of delays (τ), and
9 generating read addresses of the samples in the delay sub-lines
10 ~~(ZONE)~~ from the series of samples of the input signal ~~(INPUT)~~, so that a read
11 address is equal to a difference between a write address of a sample in a delay
12 sub-line ~~(ZONE)~~ of the input signal and a delay (τ) expressed as a number of
13 sampling periods of the series of delays (τ).